REMARKS

Claims 1 - 8, 12, 14 - 34 are pending in the present application, of which claims 15 - 34 have been withdrawn from consideration. By this Amendment, claims 2 and 36 have been amended. No new matter has been added. It is believed that this amendment is fully responsive to the Office Action dated April 23, 2003.

Allowable Subject Matter:

Applicant gratefully acknowledge the Examiner's indication in the outstanding Office Action that claims 1, 4, 12 and 14 are allowable.

Claim Rejections Under 35 U.S.C. §103

Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hosotani, et al. (USP 5,977,583) in view of Kimura (USP 6,127,734). Claims 5 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hosotani et al. in view of Kimura and Fukase (USP 5,728,596).

Both of these rejections are respectfully traversed.

The Examiner states that Hosotani shows all of the elements of the claims except the first inter-layer insulation film being in contact with the side walls of the conductor patterns. The Examiner also states that Kimura shows a semiconductor device having a first inter-layer insulation

film in contact with the side walls of the conductor patterns. According to these disclosures, the Examiner has concluded that in configuration of an inter-layer insulation film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration, so that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of Hosotani by forming the first inter-layer insulation film on the side walls of the conductor patters as taught by Kimura to simplify the manufacturing process and increase the degree of integration.

However, in Hosotani, the sidewall insulation film 21 is used as an etching stopper film for forming the self-aligned contact hole in the inter-layer insulation film 22 (see FIG. 11). When the sidewall insulation film 21 is not formed in Hosotani, the conductor patterns 18 are exposed in the contact hole, so that the self-aligned contact hole cannot be formed and the object of Hosotani cannot be achieved. Thus, in Hosotani, the sidewall insulation film 21 cannot be removed.

When the sidewall insulation film 21 is not formed, it can be considered that the contact hole is formed so as to cover the side walls of the conductor patterns 18 with the inter-layer insulation film 22, as shown in, e.g.., FIG. 1 of Kimura. However, in this case, the end of the contact hole is not defined by the conductor patterns. The sidewall insulation film is not formed in the contact hole. This structure is clearly different from the claimed inventions.

Thus, one of ordinary skill in the art would not remove the sidewall insulation film 21 of

Hosotani, even though Kimura shows a semiconductor device having the inter-layer insulation film 11 formed on the substrate in contact with the side walls of the conductor patterns.

Additionally, the sidewall insulation film of the present invention is formed on the inner wall of the contact hole and surrounding the contact hole. On the other hand, the sidewall insulation film 21 of Hosotani is formed on the whole side walls of the conductor pattern and not surrounding the contact hole. Thus, the sidewall insulation film of the present invention and that of Hosotani are clearly different from each other.

Thus, Hosotani and Kimura are clearly different from the present invention and do not provide any motivation for the present invention.

Claim 36:

Claim 36 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fukase in view of Kimura.

This rejection is respectfully traversed.

The Examiner states that Fukase shows all of the elements of the claims except the first inter-layer insulation film being in contact with the side walls of the conductor patterns. The Examiner also states that Kimura shows a semiconductor device having a first inter-layer insulation

film in contact with the side walls of the conductor patterns. According to these disclosures, the Examiner has concluded that in configuration of an inter-layer insulation film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration, so that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of Fukase by forming the first inter-layer insulation film on the side walls of the conductor patterns as taught by Kimura to simplify the manufacturing process and increase the degree of integration.

However, in Fukase, from the viewpoint of improving both the characteristics of the peripheral transistor and the contact characteristics in the memory cell region, after the sidewall insulation film 10, optimized based on the characteristics of the peripheral transistor, is removed, the sidewall insulation film 17 is again formed in the contact hole in the memory cell region (see FIGs. 2A-2G of Fukase), That is, Fukase has applied such a process on the assumption that the peripheral transistor having the LDD structure is formed. It is contrary to the premise of Fukase not to form the sidewall insulation film 10 on the side walls of the conductor patterns.

Thus, one of ordinary skill in the art would not remove the sidewall insulation film of Fukase, even though Kimura shows a semiconductor device having the inter-layer insulation film 11 formed on the substrate in contact with the side walls of the conductor patterns.

Thus, Hosotani and Kimura are clearly different from the present invention and do not provide any motivation for the present invention.

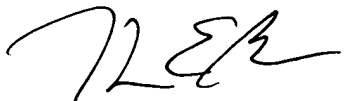
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/050,113

IN THE CLAIMS:

Claims 2 and 36 have been **AMENDED** to read as follows:

2. (Six Times Amended) A semiconductor device comprising:

a base substrate;

a first conducting film formed over the base substrate and including a plurality of conductor patterns adjacent to each other;

an etching stopper film covering an upper surface of the conductor patterns;

a contact hole located in a part of a region between the adjacent conductor patterns and having an end thereof defined by the conductor patterns;

a first insulation film ~~which is filling spaces between said plurality of conductor patterns where the contact hole is not formed,~~ formed on a rest part of the region, the first insulation film filling spaces between the adjacent conductor patterns, ~~and~~ not extending over the etching stopper film, the first insulation film being in contact with side walls of the conductor patterns; and

a sidewall insulation film formed on an inner wall of the contact hole ~~so that~~ and surrounding the contact hole, the sidewall insulation film covering the side walls of the conductor pattern and the etching stopper film ~~are covered~~ in the contact hole.

36. (Four Times Amended) A semiconductor device comprising:

a base substrate;

a first conducting film formed over the base substrate and including two conductor patterns adjacent to each other;

an etching stopper film covering each upper surface of the two conductor patterns;

a first insulation film formed over the etching stopper film and the base substrate~~, the first insulation film being in contact with the side walls of the two conductor patterns~~;

a contact hole, located between the two conductor patterns, reaching the base substrate through the first insulation film~~, wherein an end of the contact hole is positioned on the etching stopper film~~; and

a sidewall insulation film formed in the contact hole on an inner wall of the first insulation film, each side wall of the two conductor patterns, and each side wall of the etching stopper film ~~in the contact hole~~, in which

~~the~~ an end of the contact hole is defined by four sides including a first pair of sides which are opposed to each other and a second pair of sides which are opposed to each other,

the first pair of sides is defined by the conductor patterns,

the second pair of sides is defined by the first insulation film,

the sidewall insulation film does not form between the side walls of the conductor patterns and the first insulation film.